Optimization of Active Microwave Frequency Multiplier Performance Utilizing Harmonic Terminating Impedances

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ABSTRACT

A primary factor affecting optimum performance of microwave multipliers employing nonlinear devices is the proper termination of the fundamental and other harmonic frequency components. The objective of this paper is to present a *quantitative* analysis leading to the assessment of optimum terminating impedances in the design of active frequency multipliers. The analysis includes computer modeled HEMT data and supporting measured data for corresponding circuit realizations. An experimental design reveals an improvement in multiplier gain of 77% over the conventional approach.

INTRODUCTION

Numerous techniques exist for realization of frequency multipliers. At radio frequencies these techniques typically employ a nonlinear device to generate the desired frequency multiple. In the active case, the nonlinear element typically includes any of the transistor classes such as BJT, FET, etc.

In many frequency multiplier design approaches, the operating performance is improved by the proper selection of input and output circuit terminating impedances at the fundamental and harmonic frequencies. In the literature there is apparently little substantive in-depth quantitative coverage of this topic *with supporting modeled and measured data* for either BJT or FET family realizations. Various authors have given varying opinions on optimum load impedances for multiplier designs [1–5].

This paper presents a quantitative analysis of the optimization of active multiplier conversion gain and spectral purity as governed by fundamental and harmonic terminating impedances. The optimum terminating impedances are determined for the input and output ports of the active device utilizing the most current nonlinear circuit model for HEMT transistors. This is in marked contrast with earlier studies which used approximations in the simulated performance predictions [1-3,9]. Measured data are presented which validate the practicality of the designs and the accuracy of the simulation.

NONLINEAR MODEL

In analyzing FET performance, it has been found that the elements which contribute to the nonlinear behavior are the drain-source current I_{ds},the gate-source capacitance C_{gs}, gate-drain capacitance C_{gd}, output resistance R_{ds}, and diodes D_{gs} and D_{gd} [3,4,6–12]. From the construction of plots showing variations of device elements as a function of bias voltage, it may be observed that the aforementioned parameters showing the greatest nonlinearity are the transconductance g_m, gate-source capacitance C_{gs}, gate-drain capacitance C_{gd}, and output resistance R_{ds} [3,6,8,12].

The nonlinear model of the Fujitsu FHX35LG HEMT employed in this paper is shown in Figure 1 [6] (case parasitics are included in this model but not shown in Figure 1). Static I-V curves for this HEMT as obtained from the model of Figure 1 are employed to characterize the two dominant nonlinearities of the device: the transconductance (g_m) and output conductance (g_d). These parameters plotted versus the drain-to-source (V_{ds}) and gate-to-source (V_{gs}) voltages are shown in Figures 2a–b. From these plots the nonlinearity of the elements are displayed as a function of the dc bias voltages.

In this paper, rich harmonic generation is shown to result for Class A and Class B operation on the HEMT [8]. It has been shown that Class A FET multipliers provide good multiplication gain and poor DC to RF efficiency while Class B FET multipliers have poor multiplication gain and good DC to RF efficiency [8,9]. Based on the HEMT transconductance and output transconductance plots of Figures 2a-b, we are able to identify the prominent nonlinear regions for the optimum dc bias points (either V_{gs}= 0 or V_{gs} = V_p). From these curves, the prominent nonlinearity regions for V_{gs}= 0 is Region I of Figure 2a where g_d is dominant and for V_{gs} = V_p, Region II of Figure 2b with g_m showing

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the dominant effect. In the absence of embedding circuitry constraints, a preliminary conclusion on terminating impedances is developed at this juncture in the analysis. Construction of *fundamental* frequency load lines for these regions shows that Region I requires an open-circuit impedance which allows a maximum V_{ds} voltage swing and Region II requires a short-circuit impedance which allows a maximum I_{ds} current swing.

OPTIMAL DESIGN

The above analysis provides some background for determining and optimal design approach. Toward this end, a specific illustrative multiplier design is presented. The basic configuration of the frequency multiplier utilized in this paper is illustrated in Figure 3. In this configuration, $F_K - F_L$ and $F_R - F_S$ represent short-circuit terminating impedance at the respective frequencies on the input and output. Similarly, $F_M - F_N$ and $F_P - F_Q$ represent open-circuit terminating impedances at the respective frequencies on the input and output. This provides the motivation for construction of a matrix of various circuit configurations as shown in Table 1 which displays various harmonic terminating impedances on the input ad output ports fitting the configuration of Figure 3. Table 1 has been constructed for a frequency doubler utilizing the precision HEMT model with case parasitics included to illustrate the design approach. The vertical column represents various impedances of the input network at the fundamental, second harmonic, and third harmonic frequencies.

The operating performance of a HEMT frequency doubler with a fundamental frequency of 3 GHz is analyzed as a basis for comparing the present technique utilizing the configuration of Figure 3 with the traditional design approach. A "quantitative" assessment of the effects of the harmonic terminating impedances for frequency doubler operation is obta.ned utilizing a harmonic balance analysis for realizations in the topology of Figure 3. Table 1 shows the simulated output power levels of the fundamental, second, and third harmonic frequencies of the HEMT doubler operating with V_{ds} = 3V, V_{gs} = –0.7V and P_{in}= 0 dBm. A major conclusion of this analysis is that conversion gain is improved by incorporating the third harmonic terminating impedance in the design in addition to optimal fundamental and second harmonic terminations.

EXPERIMENTAL RESULTS

Conventional doubler designs have traditionally employed a short-circuit termination at the second harmonic frequency on the input network and a short-circuit termination at the fundamental on the output network. The *measured* and *simulated* results for the HEMT doubler realization utilizing this conventional approach are shown in Figure 4. The conversion gain is 5 dB at the doubler center frequency of 3 GHz, rising to 6.7 dB at 3.08 GHz. The performance of the frequency doubler designed using the techniques developed in this paper is shown in Figure 5, which shows the *measured* and *modeled* ouput power versus the fundamental frequency. This technique reveals that optimum performance is achieved with the input network terminated with 50 ohms at the fundamental and third harmonic frequencies and a short circuit at the second harmonic frequency. On the output network, a short circuit at the fundamental frequency, 50 ohms at the second harmonic frequency, and an open circuit termination at the third harmonic frequency yields optimum performance (Region II) . The resulting implementation of the technique is illustrated in Figures 5, where the realized multiplier is seen to have a conversion gain of 9 dB, fundamental suppression of ≥25 dBc, and third harmonic suppression of ≥ 50 dBc. Comparing Figures 4 and 5 shows that the optimization approach used in this paper yields and improvement of 2.5dB in the conversion gain over the conventional doubler realization.

CONCLUSION

This paper has detailed the results of an in-depth study to quantitatively determine the effects of passive circuit terminations on microwave active multiplier performance. These results show considerable improvement of frequency multiplier performance (in te rms of conversion gain and harmonic suppression) with the addition of proper terminating impedances. The optimizing technique shown in this paper demonstrates the importance in analyzing harmonic terminating impedances with special emphasis on higher-order harmonic terminations which are typically neglected in multiplier design analysis.

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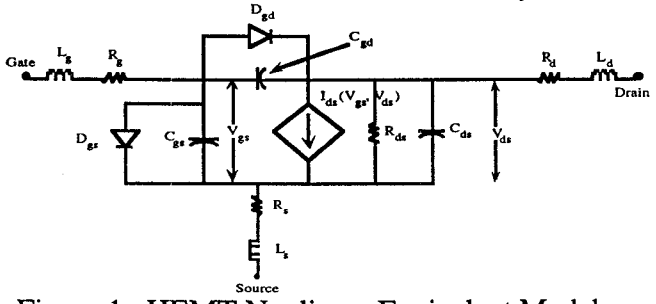

Figure 1. HEMT Nonlinear Equivalent Model

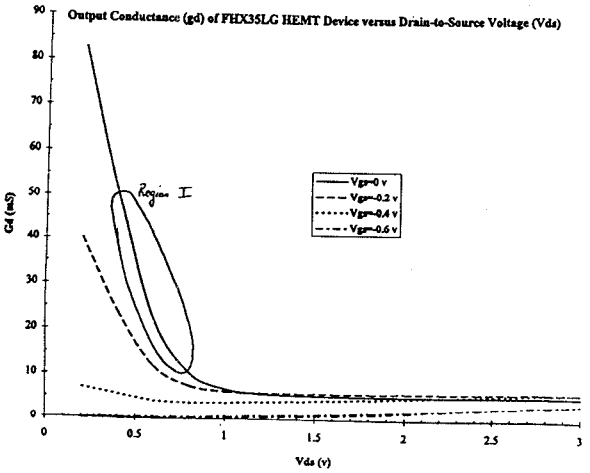

Figure 2a: FHX35LG HEMT OutputConductance versus V_{ds}

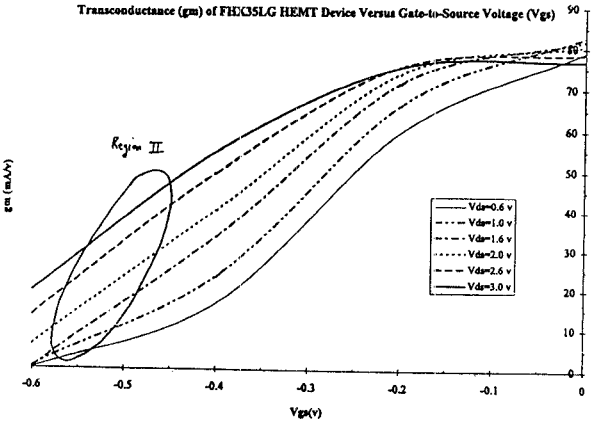

Figure 2b: FHX35LG HEMT Output Conductance vs. V_{gs}

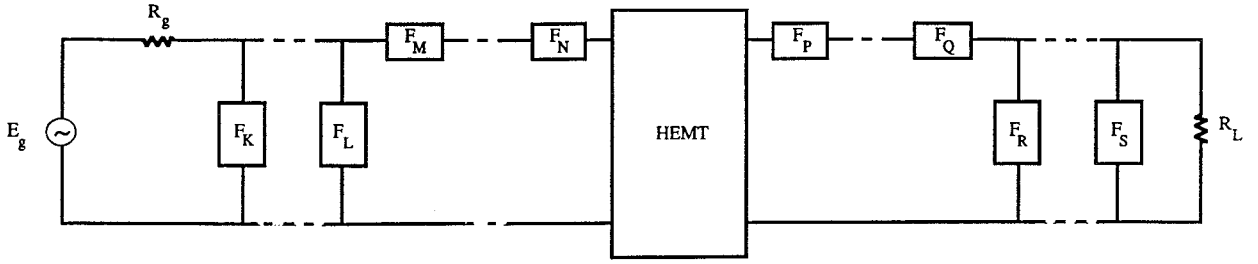

Figure 3. Frequency Multiplier Realization

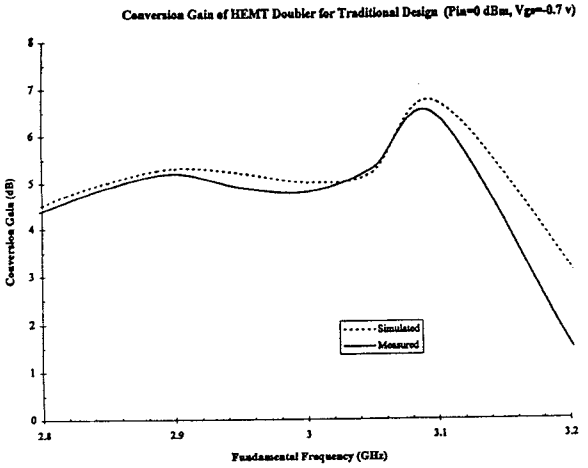

Figure 4: Conversion Gain of HEMT Doubler vs. Fundamental Frequency for Traditional Design

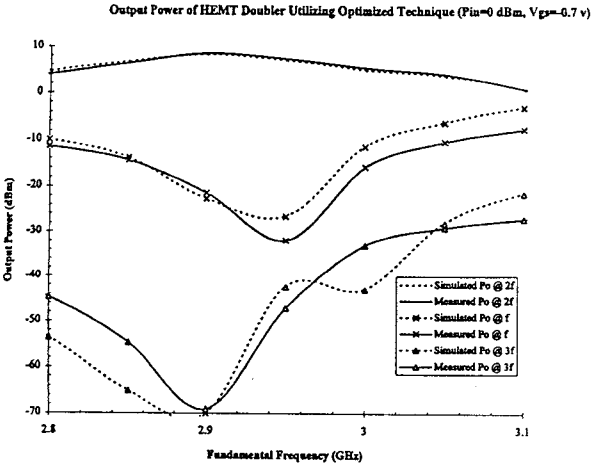

Figure 5: Output Power of HEMT Doubler vs. Fundamental Frequency Utilizing Optimization Technique

Vgs=-0.7 V Pin=0 dBm Input Network	Output Network short circuit @ fo 50 ohm @ 2fo 50 ohm @ 3fo		50 ohm @ fo 50 ohm @ 2fo open circuit @ 3fo		open circuit @ fo 50 ohm @ 2fo open circuit @ 3fo		short circuit @ fo 50 ohm @ 2fo open circuit @ 3fo	
	Output Power (dBm)		Output Power (dBm)		Output Power (dBm)		Output Power (dBm)	
50 ohm @ fo	Po @ fo	-27.1	Po @ fo	4	Po @ fo	-17.3	Po @ fo	-25
50 ohm @ 2fo	Po@2fo	-0.7	Po@2fo	0.6	Po@2fo	0.8	Po@2fo	0.4
50 ohm @ 3fo	Po@3fo	-26.3	Po@3fo	-37.7	Po@3fo	-60.1	Po@3fo	-52.9
50 ohm @ fo	Po @ fo	-27.4	Po @ fo	9	Po @ fo	-13.5	Po @ fo	-19.9
short circuit @ 2fo	Po@2fo	5.4	Po@2fo	7.2	Po@2fo	6.4	Po@2fo	7.7
50 ohm @ 3fo	Po@3fo	-22.6	Po@3fo	-32	Po@3fo	-61	Po@3fo	-46.9
50 ohm @ fo	Po @ fo	-24.5	Po @ fo	6.8	Po @ fo	-15	Po @ fo	-22.2
short circuit @ 2fo	Po@2fo	3.2	Po@2fo	5.9	Po@2fo	4.6	Po@2fo	5.5
short circuit @ 3fo	Po@3fo	-22	Po@3fo	-30.4	Po@3fo	-73.7	Po@3fo	-46

Table 1: Harmonic Impedance Terminations